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In The Claims:

Please amend the claims as follows:

Claim 1. (currently amended) A buffer device ~~message transmitting queue~~, for transmitting a plurality of messages between a source controller and a destination controller, comprising:

a plurality of message rows, for storing the messages that the source controller intends to transmit to the destination controller, each of the message rows at least comprising a write complete flag and a distribution complete flag;

a write control unit, coupled to the source controller and the plurality of message rows, used to sequentially output a plurality of free message row addresses according to the plurality of distribution complete flags, wherein when the message transmitting queue still has a free message row, the source controller reads an address of the message row that is currently free among said plurality of message rows, and the distribution complete flag of the message row that is currently free is set, and when the source controller completes writing the message of the message row that is currently free, the write complete flag of the message row that is currently free is set; and when the message transmitting queue has no free message row, said write control unit outputs a non-free message row signal; and

a read control unit, coupled to the destination controller and the plurality of message rows, to sequentially issue a read request to inform the destination controller to read the message of the message row when the write complete flag is set, wherein after the destination controller reads the message, the distribution complete flag and the write complete flag of the message row are both cleared.

Claim 2. (currently amended) The buffer device ~~message transmitting queue~~ of claim 1, wherein the write control unit comprises:

a write pointer control unit, for storing a write address of the message row that is currently free, wherein after the source controller reads the write address of the message row that is currently free, said write pointer control unit sets the distribution complete flag of the message row that is currently free and progresses the write address of the message row that is currently free, and when the source controller completes writing the message of the message row, sets the write complete flag of the message row;

a distribution complete flag multiplexer, coupled to the write pointer control unit and the distribution complete flags of the plurality of message rows, to output a not-distributed signal according to the distribution complete flag of the message row pointed to by the write address; and

a distribution address multiplexer, coupled to the distribution complete flag multiplexer and the write pointer control unit, to output the affirmative of the write address and the no free message row signal according to the not-distributed signal.

Claim 3. (currently amended) The buffer device ~~message transmitting queue~~ of claim 1, wherein the read control unit comprises:

a read pointer control unit, to store a read address of the message transmitting queue, wherein when the destination controller completes reading the message of the message row pointed to by the read address, said read pointer control unit clears the distribution complete flag and the write complete flag of the message row, and progresses the read address;

a read buffer, coupled to the read pointer control unit and the plurality of message rows, to temporarily store the message of the message row pointed to by the read address; and

a read request multiplexer, coupled to the read pointer control unit and the write complete flags of the plurality of message rows, to output the read request according to the write complete flag of the message row pointed to by the read address.

Claim 4. (currently amended) The buffer device ~~message transmitting queue~~ of claim 1, wherein each message row further comprises:

a command row, to store the command that the source controller intends to transmit to the destination controller; and

a data row, to store the data that the source controller intends to transmit to the destination controller.

Claim 5. (currently amended) The buffer device ~~message transmitting queue~~ of claim 4, wherein the size of the command row is four bytes.

Claim 6. (currently amended) The buffer device ~~message transmitting queue~~ of claim 4, wherein the size of the data row is a multiple of four bytes.

Claim 7. (currently amended) The buffer device ~~message transmitting queue~~ of claim 1, wherein the source controller is a central processing unit.

Claim 8. (currently amended) The buffer device ~~message transmitting queue~~ of claim 1, wherein the destination controller is a central processing unit.

Claim 9. (currently amended) A method for transmitting a message of a source controller to a destination controller, through a message transmitting queue having a plurality of message rows, a write pointer and a read pointer, wherein each of the plurality of message rows at least comprises a write complete flag and a distribution complete flag; said method comprises the steps of:

setting the write pointer and the read pointer to point to the first message ~~rowamong~~ row among said message rows;

the source controller reads the message of the message row pointed to by the write pointer, setting the distribution complete flag of the message row pointed to by the write pointer, and progressing the write pointer after the source controller reads the message of the message row pointed to by the write pointer;

the source controller writes the message of the message row, setting the write complete flag of the message row after the source controller writes the message of the message row;

the write complete flag of the message row pointed to by the read pointer is set, issuing a read request after the write complete flag of the message row pointed to by the read pointer is set; and

the destination controller reads the message of the message row pointed to by the read pointer, clearing the distribution complete flag and the write complete flag of the message row pointed to by the read pointer, and progressing the read pointer after the destination controller

reads the message of the message row pointed to by the read pointer.

Claim 10. (Original) The method of claim 9, wherein when the write pointer is progressed and points to a message row whose distribution complete flag is set, a no free message row signal is asserted to inform the source controller.

Claim 11. (Original) The method of claim 9, wherein the source controller is a central processing unit.

Claim 12. (Original) The method of claim 9, wherein the destination controller is a central processing unit.

Claim 13. (Original) The method of claim 12, wherein the read request is an interrupt request of the central processing unit.

Claim 14. (currently amended) A buffer device ~~message transmitting queue~~, coupled in between a source controller and a destination controller, transmitting a plurality of messages between the source controller and the destination controller, comprising:

a plurality of message rows, for storing a plurality of messages, and each of the plurality of message rows at least comprising a write complete flag and a distribution complete flag;

a write control unit having a write pointer, coupled to the source controller and the plurality

of message rows, to sequentially output the address of the free message row to the source controller to store said messages according to said distribution complete flags and said write pointer; and

a read control unit having a read pointer, coupled to the destination controller and the plurality of message rows, to sequentially issue a read request to inform the destination controller to read said messages according to said write complete flags and said read pointer.

Claim 15. (currently amended) The buffer device ~~message transmitting queue~~ of claim 14, wherein the length of each message exceeds an atomic read/write size that can be processed by said controllers.

Claim 16. (currently amended) The buffer device ~~message transmitting queue~~ of claim 14, wherein the write control unit determines whether the free message row exists according to the write pointer and the distribution complete flag of the message row pointed by the write pointer.

Claim 17. (currently amended) The buffer device ~~message transmitting queue~~ of claim 14, wherein if the write control unit determines the free message row exists, the message row address pointed to by the write pointer is returned to the source controller, the distribution complete flag of the message row pointed to by the write pointer is set, and the write pointer is incremented to point to a next message row; otherwise, a no free message row signal is returned to the source controller.

Claim 18. (currently amended) The buffer device ~~message transmitting queue~~ of claim 17, wherein when the source controller receives the no free message row signal, a request is issued to ask for the free message row from the message transmitting queue every predetermined period.

Claim 19. (currently amended) The buffer device ~~message transmitting queue~~ of claim 14, wherein after the destination controller reads a message row, the read control unit clears the distribution complete flag and the write complete flag of the message row pointed to by the read pointer, and progresses the read pointer to a next message row.

Claim 20. (currently amended) The buffer device ~~message transmitting queue~~ of claim 14, wherein when the source controller receives a free message row address, a firmware records said free message row address till an associated message has been written to the free message row address completely.